Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1. (currently amended) A circuit comprising:

a sigma-delta converter portion that outputs a digital data stream with a digital amplitude, the digital data stream being N bits wide in a first mode and M bits wide in a second mode, wherein the sigma-delta converter portion includes a sigma-delta modulator and a filter; and

a post converter filter portion that receives the digital data stream, the post converter filter portion having a cut-off frequency that is determined at least in part based on the digital amplitude of the digital data stream.

2. (original) The circuit of claim 1, wherein the digital data stream is a series of multi-bit digital values, each multi-bit digital value having N bits in the first mode and M bits in the second mode, wherein the series of multi-bit digital values has 2N different digital values in the first mode and 2M different digital values in the second mode, and wherein the digital amplitude at a given point in time is one of the multi-bit digital values.

3. (original) The circuit of claim 1, wherein in the first mode, the post converter filter portion has a first cut-off frequency when the digital amplitude of the digital data stream is in a first amplitude range, and the post converter filter portion has a second cut-off frequency when the digital amplitude of the digital data stream is in a second amplitude range.

4. (original) The circuit of claim 3, further comprising:

a register that stores a reference value corresponding to the digital amplitude at a boundary between the first amplitude range and the second amplitude range.

5. (original) The circuit of claim 4, further comprising:

a processor, wherein the register is writable by the processor.

6. (original) The circuit of claim 3, wherein the sigma-delta converter portion has a digital low-pass filter having a fixed cut-off frequency, wherein the first cut-off frequency of the post converter filter portion is higher than the fixed cut-off frequency, and wherein the second cut-off frequency of the post converter filter portion is lower than the fixed cut-off frequency.

7. (original) The circuit of claim 1, wherein the sigma-delta converter portion comprises a sigma-delta modulator and a digital low-pass filter.

8. (original) The circuit of claim 1, wherein post converter filter portion comprises a variable low-pass filter, and wherein the variable low-pass filter is an infinite impulse response digital filter.

9. (original) The circuit of claim 1, wherein the circuit is an integrated circuit.

10. (original) The circuit of claim 1, wherein the post converter filter portion includes a variable low-pass filter, the variable low-pass filter being controlled by a digital filter control value, the digital filter control value being determined at least in part based on the digital amplitude of the digital data stream.

11. (original) The circuit of claim 1, wherein the digital data stream has a noise level, and wherein the cut-off frequency of the post converter filter portion is determined at least in part based on the noise level of the digital data stream.

12. (original) The circuit of claim 11, wherein the noise level of the digital data stream is calculated based on an average deviation of a predetermined number of the multi-bit digital values of the digital data stream.

13. (original) The circuit of claim 1, wherein M is larger than N, and wherein the cut-off frequency in the first mode when the digital amplitude equals A is the same as the cut-off frequency in the second mode when the digital amplitude has a value that is greater than A.

14. (original) A method, comprising:

receiving a digital data stream from a sigma-delta converter portion, the digital data stream having a digital amplitude and containing noise;

setting a cut-off frequency of a variable filter of a post converter filter portion based at least in part on the digital amplitude of the digital data stream; and

passing the digital data stream through the variable filter such that the post converter filter portion filters out a portion of the noise.

15. (original) The method of claim 14, wherein the digital data stream is N bits wide in a first mode and M bits wide in a second mode, and wherein the cut-off frequency in the first mode when the digital amplitude equals A is the same as the cut-off frequency in the second mode when the digital amplitude equals A times M divided by N.

16. (original) The method of claim 15, further comprising:

programming a value for N and a value for M.

17. (original) The method of claim 14, wherein the setting the cut-off frequency comprises:

writing a reference value to a register, wherein the reference value corresponds to a boundary of an amplitude range.

18. (original) The method of claim 14, wherein the setting the cut-off frequency comprises:

determining the digital amplitude of the digital data stream; and

comparing the digital amplitude to a boundary of an amplitude range.

19. (original) The method of claim 14, wherein the digital data stream has a noise level, and wherein the setting the cut-off frequency is based at least in part on the noise level of the digital data stream.

20. (original) A sigma-delta analog-to-digital converter, comprising:

a sigma-delta converter portion that outputs an intermediary digital data stream of multi-bit digital values, each of the multi-bit digital values having N bits, the intermediary digital data stream having noise; and

means for receiving the intermediary digital data stream and for outputting a digital data stream of multi-bit digital values such that the digital data stream has less noise than the intermediary digital data stream, wherein each of the multi-bit digital values of the digital data stream has N bits, and wherein the means is programmable to receive the intermediary digital data stream in a first mode for which N is a first value and in a second mode for which N is a second value.

21. (original) The sigma-delta analog-to-digital converter of claim 20, wherein each of the intermediary digital data stream and the digital data stream has 2N possible digital values.

22. (original) The sigma-delta analog-to-digital converter of claim 20, wherein the means comprises:

means for analyzing a digital amplitude of the intermediary digital data stream and for outputting a filter control value; and

a variable filter that receives the filter control value from the means for analyzing.

23. (original) The sigma-delta analog-to-digital converter of claim 20, wherein the means filters the intermediary digital data stream with a variable filter.